ABSTRACT OF THE DISCLOSURE

PSEUDO-DIFFERENTIAL PARALLEL SOURCE SYNCHRONOUS BUS

The present invention provides a bus for use in a data processing system. In one embodiment, the bus includes a clock driver, a clock receiver, a plurality of drivers, and a plurality of receivers. The clock receiver is coupled to the clock driver by two clock bus lines carrying complementary clock pulses. Each of the plurality of receivers each coupled to a respective one of the plurality of drivers by bus lines, wherein the receivers detect signals on respective bus lines with respect to a reference voltage derived from a combination of the complementary clock pulses.